# PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
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# PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

| | |
|---|---|
| Date of mailing *(day/month/year)* | 15 AUG 2008 |
| Applicant's or agent's file reference<br>5087-1082 | **FOR FURTHER ACTION**<br>See paragraph 2 below |

| International application No. | International filing date *(day/month/year)* | Priority date *(day/month/year)* |
|---|---|---|
| PCT/US 08/60680 | 17 April 2008 (17.04.2008) | 17 April 2007 (17.04.2007) |

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - G06F 7/38 (2008.04)
USPC - 326/38

Applicant CYPRESS SEMICONDUCTOR CORPORATION

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

| Name and mailing address of the ISA/US | Date of completion of this opinion | Authorized officer: |
|---|---|---|
| Mail Stop PCT, Attn: ISA/US<br>Commissioner for Patents<br>P.O. Box 1450, Alexandria, Virginia 22313-1450<br>Facsimile No. 571-273-3201 | 04 August 2008 (04.08.2008) | Lee W. Young<br>PCT Helpdesk: 571-272-4300<br>PCT OSP: 571-272-7774 |

**WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY**

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**Box No. I Basis of this opinion**

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. type of material

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing

      ☐ contained in the international application as filed

      ☐ filed together with the international application in electronic form

      ☐ furnished subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

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**Box No. V** **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

| | | | |
|---|---|---|---|
| Novelty (N) | Claims | 1 - 20 | YES |
| | Claims | None | NO |
| Inventive step (IS) | Claims | None | YES |
| | Claims | 1 - 20 | NO |
| Industrial applicability (IA) | Claims | 1 - 20 | YES |
| | Claims | None | NO |

2. Citations and explanations:

Claims 1-20 lack inventive step under PCT Article 33(3) as being obvious over US 6,864,710 B1 to Lacey et al. (hereinafter 'Lacey') in view of US 2004/0017222 A1 to Betz et al. (hereinafter 'Betz').

As to claims 1, 12, and 18, Lacey teaches an apparatus, integrated circuit, and method, comprising: an array of digital blocks (Col. 3 ln. 16 -37); and a programmable interconnect matrix including segmentation elements (logic elements) that programmably interconnect different horizontal channels together (Col. 3 ln. 24-27; Col. 4 line 20-41). Lacey does not explicitly teach horizontal channels that programmably couple different groups of one or more digital blocks together. However, Betz teaches horizontal channels that programmably couple different groups of one or more digital blocks together (para. [0015], [0020] and [0021]). It would have been obvious to one skilled in the art to combine the teachings of Lacey with those of Betz in order to, in a PLD architecture, optimize a selected one or more operation parameters, while minimizing the impact on the remaining parameters.

As to claims 2, and 13, Lacey teaches the invention wherein the segmentation elements include: horizontal segmentation switches that programmably couple together the horizontal channels in a same row; and vertical segmentation switches that programmably couple together the horizontal channels in different rows (Col. 3 ln. 16-20).

As to claim 3, Lacy teaches the invention further comprising vertical channels that programmably interconnect the horizontal channels in different rows, wherein the horizontal channels provide more connectivity between the digital blocks located in the same, rows than connectivity provided by the vertical channels between the digital blocks located in different rows (Col. 9 ln. 1-20).

As to claim 4, Betz teaches the invention wherein two digital blocks in a same digital block pair are tightly coupled together to common routes in a same associated horizontal channel and different digital block pairs are less tightly coupled together through the segmentation elements (para. [0012] and [0017]).

As to claims 5, and 15, Betz teaches the invention further comprising: programmably selectable channel switches configured to connect different selectable signals from the digital bocks to associated horizontal channels; and programmable tri-state buffers in the segmentation elements configured to selectively couple together and drive signals between the different horizontal channels (para. [0020] and [0021]).

As to claim 6, Betz teaches the invention further comprising a Random Access Memory (RAM) configured to programmably control how the different digital blocks are coupled together through the interconnection matrix (para. [0006]).

As to claim 7, Lacey teaches the invention including Inputs and Outputs (I/Os) that are initially not dedicated to any particular digital blocks and that are programmably coupled to different selectable digital blocks through different selectable routes in the interconnect matrix (Col. 2 ln. 12-31).

As to claim 8, Lacey teaches the invention further comprising a micro-controller system programmab1y coupled to the different digital blocks and to different selectable Inputs/Outputs (I/Os) through the interconnect matrix (Col. 4 ln. 8-19).

As to claim 9, Lacey teaches the invention the micro-controller system includes a micro-controller, an interrupt controller, and Direct Memory Access (DMA) controller; interrupt requests are programmably coupled between the interrupt controller and different selectable digital blocks or different selectable I/Os through the interconnect matrix; and DMA requests are programmably coupled between the DMA controller and different selectable digital blocks or different selectable I/Os through the interconnect matrix (Col. 2 ln. 12-31).

As to claim 10, Lacey teaches the invention wherein the micro-controller system, digital blocks, I/Os, and interconnect matrix are all located in a same integrated circuit Col. 3 ln. 16-37.

As to claim 11, Betz teaches the invention wherein the digital blocks each comprise a first group of uncommitted logic elements that are programmable into different logic functions and a second group of dedicated logic elements that together form a programmable arithmetic sequencer (para. [0015]).

---Please See Continuation Sheet---

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**Supplemental Box**

**In case the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box No. V
2. Citations and explanations:

As to claim 14, Lacey teaches the invention further comprising: programmably configurable digital blocks that are selectively coupled to the horizontal channels according to bits loaded into the memory device (Col. 3 ln. 33-37).

As to claim 16, Lacey teaches the invention further comprising undedicated external Input and Output pins that are programmably coupled to different inputs and outputs in the micro-controller system through the programmable interconnect and also programmably coupled to different selectable functional elements in the different digital blocks through the programmable interconnect (Col. 2 ln. 12-31).

As to claim 17, Lacey teaches the invention wherein the micro-controller system further comprises: an interrupt controller that receives interrupt requests through the programmable interconnect from different selectable digital blocks or different selectable I/Os; and a Direct Memory Access (DMA) controller that receives DMA requests through the programmable interconnect from different selectable digital blocks or different selectable I/Os (Col. 2 ln. 12-31).

As to claim 19, Betz teaches the invention further comprising: writing a first set of values into a configuration memory that control connections between the functional elements and the associated local routing channels; writing a second set of values into the configuration memory that control the interconnections between different local routing channels; and writing a third set of values into the configuration memory that control the interconnections between the local routing channels and the general routing channels (para. [0006], [0015], [0020] and [0021]).

As to claim 20, Betz teaches the invention further comprising: programming different paths through the interconnect matrix that connect different external pins or different internal functional elements to a same interrupt line on an internal interrupt controller; or programming different paths through the interconnect matrix that connect different external pins or different internal functional elements to a same Direct Memory Access (DMA) line on an internal DMA controller ([0015], [0020] and [0021]).

Claims 1-20 have industrial applicability as defined by PCT Article 33(4) because the subject matter claimed can be made or used in industry.